CUSTOMER NO.: 24498
Serial No.: 10/518,670
Date of Office Action: 10/16/07
Response dated: 01/23/08

Amendments to the Specification

Please amend the specification as follows:

Please insert the following paragraph as the second paragraph under the heading "Cross Reference" on page 1 above line 15 as follows:

This application expressly incorporates by reference herein, as if reproduced in its entirety, co-pending U.S. Patent Application Serial No. 10/518,226 (Atty. Docket No. IU020160), filed on even date herewith and assigned to the Assignee of the present application.

Please amend the following paragraph beginning on page 5, line 19 as follows:

From the input selection circuitry 123, the N input digital audio data streams are propagated to the parity encoder circuits 126. The parity encoder circuit processes the data received thereby to include parity information. It is contemplated that a wide variety of algorithms may be used to encode the received input digital audio data streams with parity information. For example, the first and second parity encoder circuits 126a and 126b may be configured to add a byte of parity information to each data frame and a frame of parity information for each 32 input data streams in the manner described and illustrated in co-pending U.S. Patent Application Ser. No. ~~10/~~ 10/518,226 (Atty. Docket No. IU010620) and previously incorporated by reference. It should be noted, however, that when using the aforementioned technique, the number of parity encoded data streams output the parity encoder circuit 126 will vary based upon the number of input data streams. For example, using the aforementioned technique, the parity encoder 126 will produce 264 parity encoded data streams from 256 input data streams. Of course, the techniques disclosed in the above-referenced patent application is but one of a wide variety of suitable techniques for encoding data with parity information. Other

- 2 -

techniques, for example, cyclic redundancy check (or "CRC") or checksum, are suitable for the purposes contemplated herein.

Please amend the following paragraph beginning on page 6, line 12 as follows:

From the parity encoder 126, parity encoded digital audio data streams 1 through N are propagated to both a first router matrix 124a which resides on the first router matrix card 122a and to a second router matrix 124b which resides on the second router matrix card 122b. Additionally, the first and second router matrices 124a and 124b receive input digital audio data streams N+1 through 2N from the second broadcast router component 104, input digital audio data streams 2N+1 through 3N from the third broadcast router component 106 and input digital audio data streams 3N+1 through 4N from the fourth broadcast router component 108. Of course, input digital audio streams N+1 through 4N are all parity encoded, preferably prior to transmission to the first router matrix 124a of the first router matrix card 122a and to the second router matrix 124b of the second router matrix card 124b. While it is fully contemplated that a variety of broadcast router configurations which include plural router matrices having identical inputs to each router matrix would be suitable for the purposes contemplated herein, one such broadcast router is disclosed in co-pending U.S. Patent Application Ser. No. ~~10/~~~~_____~~ 10/518,226 (Atty. Docket No. IU020160) and previously incorporated by reference. In that application, a broadcast router having four broadcast router components, each including a pair of router matrices coupled to receive input digital audio data streams 1 through 4N is described in great detail.

CUSTOMER NO.: 24498
Serial No.: 10/518,670
Date of Office Action: 10/16/07
Response dated: 01/23/08

PATENT
PU020289

Please amend the following paragraph beginning on page 8, line 19 as follows:

Residing on the output card 128 are a first parity check circuit 130a, a second parity check circuit 130b, a first delay circuit 132a, a second delay circuit 132b, a logic circuit 134 and a switching circuit 136. From the first parity encoder circuit 126a, the parity encoded digital audio data streams, are propagated to both the parity check circuit 130a and the delay circuit 132a. The first delay circuit 132a delays propagation of the received parity encoded digital audio data streams while the first parity check circuit 130a checks the received parity encoded digital audio data streams for the presence of a transmission error. While the first delay circuit 132 may be variously configured, it is contemplated that a first-in-first-out (or "FIFO") memory device having a width corresponding to the number or received parity encoded digital audio data streams and a depth selected based upon the time required for the parity check circuit 130a to perform the desired parity checks, for example, the parity checks described in the aforementioned U.S. Patent Application Ser. No. ~~10/~~ 10/518,226 (Atty. Docket No. IU010620), on the received parity encoded digital audio data streams. Similarly, from the parity encoder circuit 126b, the replicated parity encoded digital audio data streams are propagated to both the parity check circuit 130b and the delay circuit 132b. Here, the second delay circuit 132b delays propagation of the replicated received parity encoded digital audio data streams while the second parity check circuit 130b checks the received replicated parity encoded digital audio data streams for the presence of a transmission error.

- 4 -

Please amend the following paragraph beginning on page 10, line 11 as follows:

As disclosed herein, once the output of the broadcast router component 102 has been switched to the second parity encoded digital audio stream, the selector circuit 136 will continue to pass the second parity encoded digital audio data stream output the first second delay circuit 132b whether or not the transmission error detected in the first parity encoded digital audio data stream clears. Thus, once the second parity encoded digital audio stream has been selected by the selector circuit 136, the first parity encoded digital audio data stream output the first delay circuit 132a will remain unselected. If, however, the second parity check circuit 130b subsequently detects an error in the second parity encoded digital audio data stream, the second parity check circuit 130b will assert the output 138b. In response, the logic circuit 134 will deassert the output 140, thereby causing the selector circuit 136 to deselect the second parity encoded digital audio stream and to reselect the ~~second~~ first parity encoded digital audio stream as the output of the broadcast router component 102.

- 5 -